

CORNERSTONE DESIGN GUIDELINES

ePIXfab Silicon Photonic Summer School 2026



SIGN-UP DEADLINE: 10/07/2026

DESIGN SUBMISSION DEADLINE: 24/07/2026

All deadlines end at 13:00 (UK time)

1 TERMS AND CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms. Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

This run is part of ePIXfab Silicon Photonics Summer School, set to be organised between 22-26 June 2026. No submissions from outside of the course participation list will be accepted.

We are excited to introduce our new CORNERSTONE customer portal, beta launching with the ePIXfab Silicon Photonics Summer School Design Competition. This streamlined platform will allow you to view your quote, and upload your design submission and purchase order all in one place. To sign up for the competition, please visit:

<https://cornerstone.sotonfab.co.uk/mpw/cornerstone-epixfab2026/>

Keep an eye out for your portal invitation link shortly after submitting your project details.

The access fees are detailed in Table 1 below.

Table 1: Design area and access cost

Design Area [mm ²]	6 x 3
Access Cost*	£120

**Quoted prices include shipping, but are exclusive of VAT, import duties/customs fees and withholding taxes.*

1.1 FILE FORMAT

Designs must be submitted in a Graphical Database System file format (extension .gdsII). Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file. We recommend dedicated lithography editing software be used in the design of the .gdsII file.

2 PROCESS FLOW

For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate with resistivity of 750 $\Omega\cdot\text{cm}$
- Thermal silica (SiO_2) **B**uried **O**Xide (BOX) layer with a thickness $h_{\text{BOX}} = 2\text{ }\mu\text{m}$
- Crystalline Silicon (Si) core layer (100)-oriented with a thickness $h_{\text{wg}} = 220 \pm 20\text{ nm}$

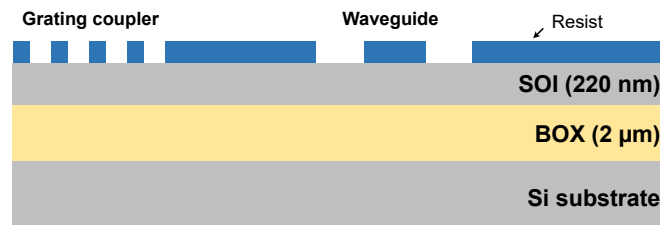
We offer a single silicon etch of $120 \pm 10\text{ nm}$. We will deposit a $1\text{ }\mu\text{m} \pm 100\text{ nm}$ -thick silicon dioxide top cladding layer after silicon etching.

The schematic description of the process flow is given below:

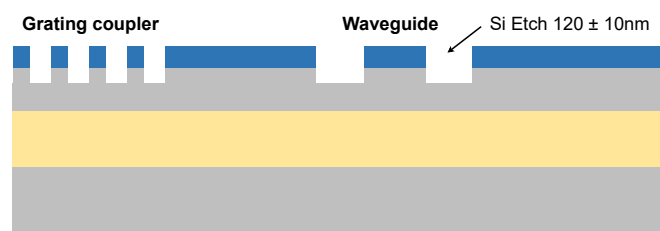
1. Starting SOI substrate



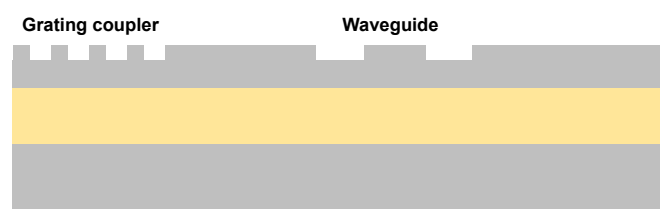
2. Resist patterning for SOI Etch (GDS layer 3 & 4) – $120 \pm 10\text{ nm}$ etch



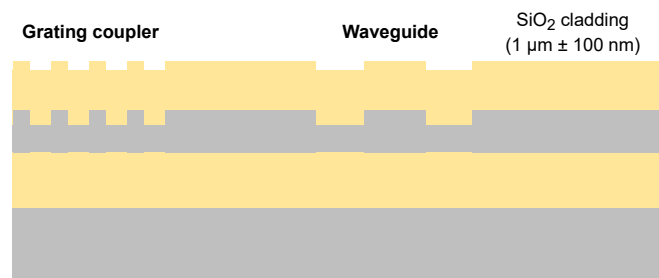
3. Shallow Si etch ($120 \pm 10\text{ nm}$ etch depth)



4. Resist strip



5. Deposition of $1\ \mu\text{m} \pm 100\ \text{nm}$ -thick SiO_2 top cladding



3 DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

3.1 DESIGN AREA

The standard user cell has dimensions of $6 \times 3\ \text{mm}^2$. Each student will receive a single $25 \times 33\ \text{mm}^2$ that contains their designs, in addition to all the designs from other partners in the course, with a schematic of where to find their own design. An illustration is shown below in Figure 1.

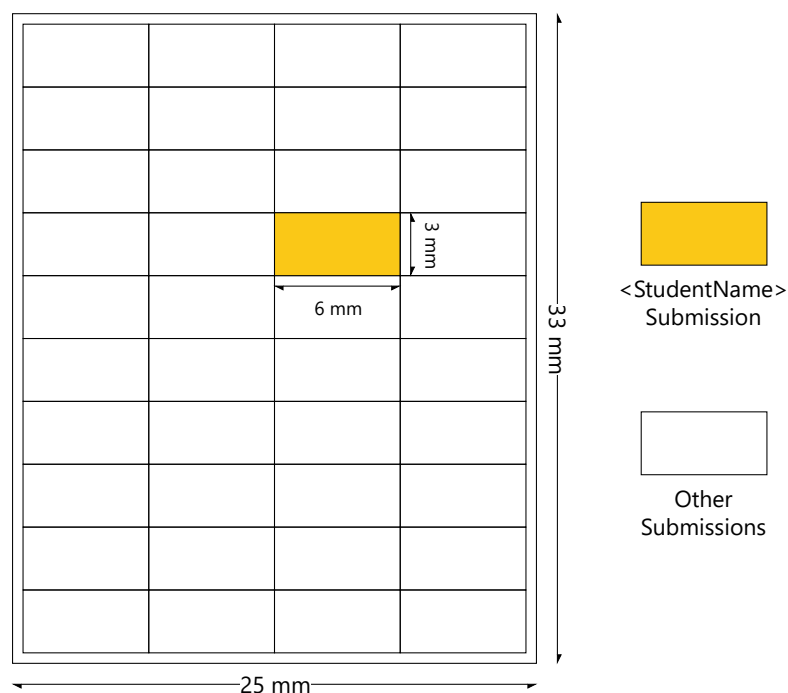


Figure 1: Exemplary user information sheet with corresponding placement indicated. Physical die size and individual payload area is marked for user information.

3.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Process layer(s): Patterns on these layers will be transferred (directly or indirectly) onto the chips during fabrication.

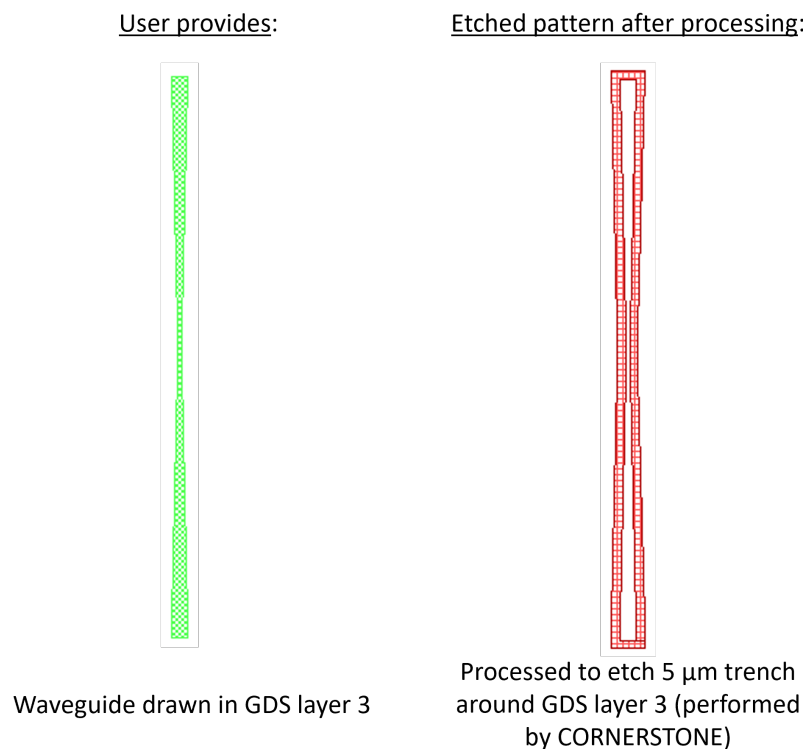


Figure 2: Description of GDS Layer 3 processing.

Silicon Etch (Waveguide layer) – etch depth: 120 ± 10 nm:

This layer defines rib waveguides and grating couplers, and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3 (Light field):

Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching. During fracturing processing, this will be translated into a pattern that defines 5 μm-wide trenches on either side of the waveguides drawn in GDS Layer 3 (see Figure 2).

GDS Layer 4 (Dark field):

Drawn objects on this layer will be exposed to the 120 nm silicon etch. The layer can be used for structures such as labels and grating couplers.

Labels – GDS Layer 100: This layer defines text labels, which will be merged with Silicon Etch layer by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Information layer(s): These layers are purely informative and their contents will not be transferred onto the chips during fabrication.

Cell Outline – GDS Layer 99: This layer defines the design space boundaries (6 x 3 mm²).

3.3 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed below.

Table 2: Design Rules Summary

Layer Description	GDS Number	Field	Min. Feature Size	Min. Gap	Max. Feature Length
Silicon Etch	3/0	Light	250 nm	200 nm	20 µm
			300 nm	200 nm	N/A
	4/0	Dark	200 nm	250 nm	20 µm
			200 nm	300 nm	N/A
Cell Outline	99/0	N/A	N/A	N/A	N/A
Labels*	100/0	Dark	250 nm	250 nm	N/A

**Features drawn in the Labels layer will be merged into Silicon Etch Layer by the CORNERSTONE team.*

A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

3.4 GDSII TEMPLATE FILE

A .gdsII template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

3.5 KLAYOUT DESIGN RULE CHECK

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE in the design documentation package. Note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail. It is critical that your submitted mask design does not contain any DRC violations, otherwise it will not be accepted for fabrication and you will have no opportunity to correct it.

4 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design, you must first sign-up to this call using the online form found using the link below.

<https://cornerstone.sotonfab.co.uk/mpw/cornerstone-epixfab2026/>

After signing up, you will receive an invitation to register for the CORNERSTONE customer portal, where you can upload your designs and the corresponding purchase orders. The sign-up deadline is found at the top of this document.

Please ensure that the top cell in your design file is titled 'Cell0_[Name of Institution]'. This helps us identify the intended design within the hierarchy of the file, and allows us to streamline the post-processing & tapeout flows.

5 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your .gdsII file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 3.2.

Silicon Etch GDS 3 (Light field) & GDS 4 (Dark field) – waveguides:

1. Grow Waveguide layer (GDS Layer 3) by 5 μm in all directions.
2. Subtract the Waveguide layer (GDS Layer 3) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Silicon Etch 2 layer (GDS Layer 4) and the Labels layer (GDS Layer 100).

6 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact your course instructor or supervisor.